LEE – 10/743,454
Client/Matter: C21906-0307405

REMARKS

Claim 1 is pending. By this Amendment, claim 1 is amended, and claims 2-4 are cancelled. No new matter is added. Reconsideration in view of the above-outlined amendments and the following remarks are respectfully requested.

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,395,635 to Wang et al. ("Wang '635"). Claims 3 and 4 were rejected under 35 U.S.C. § US Patent Publication No. 2003/0003745 to Wang et al. ("Wang '745"). These rejections are respectfully traversed.

Amended claim 1 is directed to a method for planarizing a surface of a semiconductor wafer. The method planarizes a surface of semiconductor wafer without causing scratches thereon. The method includes depositing an insulator layer on the semiconductor wafer. The insulator layer is an inter metal dielectric layer made of fluorinated silicate glass, undoped silicate glass, tetraethoxysilicate or SiH. The method further includes performing a first polishing process on a surface of the insulator layer deposited on the semiconductor wafer while supplying slurry to the surface of the insulator layer to polish about 80% thickness of a total polishing target of the insulator layer. The method also includes performing a second polishing process on the surface of the insulator layer while supplying water to the surface of the insulator layer to polish the remainder of the insulator layer. Wang '635 and Wang '745 fail to disclose the subject matter of the present invention.

Wang '635 discloses a chemical mechanical planarization process for the reduction of tungsten damascene residue and the elimination of surface scratch within the surface that is being polished. Wang '635 discloses a three step polishing sequence of the inter level dielectric followed by a two step buffing procedure of the inter level dielectric. The sequence includes applying de-ionized water, an oxide slurry and de-ionized water polishing. he three step polishing procedure reduces the device defect count by eliminating damascene residue from the polished surface. The two step buffing procedure reduces micro scratch within the polished surface thus improving device throughput.

While Wang '635 includes both water and slurry polishing, Wang '635 does not disclose the claimed invention. The polishing sequence in Wang '635 differs from that of the present invention. The present invention prevents scratches on the semiconductor wafer by removing slurry residue by a water polishing process after a slurry polishing process. Wang '635 uses the polishing procedure to reduce the device defect count by eliminating

damascene residue from the polished surface. The two step buffing procedure in Wang '635 is used to reduce micro-scratches by means of removing approximately 1000Å of oxide. In the outstanding Office Action, the Examiner takes the position that the polishing process using water prior to the polishing process with slurry in Wang '635 is a cleaning process. The Examiner further states that a cleaning step must be done after each processing step in the fabrication sequence. Under such an interpretation, the water polishing process performed by Wang '635 after the slurry polishing must also be considered a cleaning process. As such, Wang '635 does not disclose the claimed two step polishing process. Instead, under the Examiner's interpretation of Wang '635, Wang '635 discloses a one step polishing process using slurry. Since Wang '635 discloses only a single polishing step based upon the Examiner's interpretation of Wang '635 or a three step polishing process based upon the disclosure of Wang '635, Wang '635 fails to disclose polishing about 80% thickness of a total polishing target of an insulator layer during a first polishing process using slurry, and polishing about 20% thickness of the total polishing target of the insulator layer by performing a second polishing process using water instead of slurry. This is not disclosed, taught or suggested by Wang '635. Experimentation using either the "one step" or "three step" Wang '635 process would not lead one of ordinary skill in the art to obtain the polishing targets for the claimed two step process of the present invention. Accordingly, the claimed method is not obvious in view of Wang '635. Finally, Wang '635 fails to disclose that the insulator layer is an inter metal dielectric layer made of FSG, USG, TEOS or SiH which can be polished by water.

The Office Action relies upon Wang '745 for allegedly teaching that an inter metal dielectric may be made of TEOS. Wang '745, however, fails to teach any of the other deficiencies in Wang '635, discsussed above. Futhermore, wang '745 provides no teaching that the material of the inter metal dielectric must be polished by water. Applicant respectfully submits that the combination of Wang '635 and Wang '745 fails to render obvious the subject matter of the claimed invention. Applicant respectfully submits that Wang '635 and Wang '745 fail to disclose, teach or suggest the subject matter of claim 1. Claim 1 is in condition for allowance. Reconsideration and withdrawal of the rejections are respectfully requested.

Applicant respectfully submits that claim 1 defines subject matter that is patentable over the prior art of record. Should any issues require further resolution, the Examiner is requested to telephone applicant's undersigned attorney to discuss and resolve these issues.

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Reconsideration and allowance of the above-identified application in view of the following remarks are respectfully requested. Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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